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EXAMINER	
WENDELL, ANDREW	
ART UNIT	**PAPER NUMBER**
2618	

DATE MAILED: 12/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,327	SUH ET AL.	
	Examiner	Art Unit	
	Andrew Wendell	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *05 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/5/2006 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-6, 21, 25-26, 30-31, 35-36, 40, and 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Woods et al. (US Pat# 6,101,566).

Regarding claim 1, Funk et al. wireless packet data communication modem teaches a central processing unit 421 (Fig. 4) electrically connected to A address lines and M data lines of a processor bus 430, 432, and 434 (Fig. 4), wherein the A address lines convey A bits of an address in parallel (it is pretty well know there is address lines since the modem is being connected to a computer and in figure 4shows the lines being in parallel) and the M data lines convey M bits of data in parallel (Fig. 5 shows that

packet data is sent though the bus to the controller interface); a packet bus having: control lines for conveying control signals (Col. 5 lines 4-7 and Fig. 5); and N bidirectional data lines for conveying a command packet and for conveying a data packet including the M its of data, wherein each of A and M is greater than N, and wherein A, M, and N are integers (it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore A and M is greater than N); and a master controller 111 (Fig. 4, Col. 3 lines 26-30), electrically connected to the A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of the packet bus, for controlling via the packet bus a plurality of peripherals 425 (Fig. 4) electrically connected to the control lines and the N bidirectional data lines of the packet bus. Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above. Also, Funk et al. fails to clearly teach where there is address lines even though it is pretty well known as explained above.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more A address (Col. 8 lines 37-38, there is address lines as being the "other signal lines") and M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2). Also, lines 1.17 (Fig. 2) are in parallel, so the address and data lines are in parallel.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate M data lines is

greater than N data lines as taught by Dias et al. into Funk et al. wireless packet data communication modem in order to have a more compact circuit (Col. 7 lines 25-30).

Funk and Dias fail to teach address lines

Woods's system teaches A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel (Col. 1 lines 60-62 and Col. 4 lines 3-7).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate address lines as taught by Woods into M data lines is greater than N data lines as taught by Dias et al. into Funk et al. wireless packet data communication modem in order to simplify logic to interference (Col. 3 lines 44-59).

Regarding claim 2, Funk further teaches wherein the mater controller includes packet generator configured to packetized the M bits of data received in parallel through the M data lines of the processor bus, the M bits of data being thereby formatted to be conveyed via the N directional data lines of the packet bus (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Regarding claim 5, the combination including Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a command packet commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the N bidirectional data lines of the packet bus 430, 432, and 434 (Fig. 4), wherein the command packet includes a module device select signal for selecting one of the plurality of peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 6, the combination including Funk et al. teaches wherein the selected one of the plurality of peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the command packet (Col. 7 lines 48-54).

Regarding claim 21, Funk et al. wireless packet data communication modem teaches a central processing unit 421 (Fig. 4) electrically connected to A address lines and M data lines of a processor bus 430, 432, and 434 (Fig. 4), wherein the A address lines convey A bits of an address in parallel (it is pretty well know there is address lines since the modem is being connected to a computer and in figure 4shows the lines being in parallel) and the M data lines convey M bits of data in parallel (Fig. 5 shows that packet data is sent though the bus to the controller interface); and a first master controller 111 (Fig. 4, Col. 3 lines 26-30), electrically connected to the A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of the first packet bus, for controlling via the packet bus a plurality of peripherals 425 (Fig. 4) electrically connected to the control lines and the N bidirectional data lines of the first packet bus; wherein the first packet bus includes: control lines for conveying control signals (Col. 5 lines 4-7 and Fig. 5); and N bidirectional data lines for conveying a command packet and for conveying a data packet including the M its of data, wherein each of A and M is greater than N, and wherein A, M, and N are integers (it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore A and M is greater than N). Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above.

Also, Funk et al. fails to clearly teach where there is address lines even though it is pretty well known as explained above.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more A address (Col. 8 lines 37-38, there is address lines as being the "other signal lines") and M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2). Also, lines 1.17 (Fig. 2) are in parallel, so the address and data lines are in parallel.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate M data lines is greater than N data lines as taught by Dias et al. into Funk et al. wireless packet data communication modem in order to have a more compact circuit (Col. 7 lines 25-30).

Funk and Dias fail to teach address lines

Woods's system teaches A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel (Col. 1 lines 60-62 and Col. 4 lines 3-7).

Regarding claim 25, Funk et al. further teaches wherein the first master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a command packet commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the N bidirectional data lines of the packet bus 430, 432, and 434 (Fig. 4).

Regarding claim 26, Funk et al. further teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the command packet (Col. 7 lines 48-54).

Regarding claim 30, Funk further teaches wherein N is four (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Regarding claim 31, Funk et al. wireless packet data communication modem teaches a central processing unit 421 (Fig. 4) electrically connected to A address lines and M data lines of a processor bus 430, 432, and 434 (Fig. 4), wherein the A address lines convey A bits of an address in parallel (it is pretty well know there is address lines since the modem is being connected to a computer and in figure 4shows the lines being in parallel) and the M data lines convey M bits of data in parallel (Fig. 5 shows that packet data is sent though the bus to the controller interface); and a second packet bus 432 (Fig. 4) having control lines and N data lines for conveying a command packet and a data packet including the M bits of data; and a master controller 111 (Fig. 4, Col. 3 lines 26-30), electrically connected to the A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of the packet bus, for controlling via the packet bus a plurality of peripherals 425 (Fig. 4) electrically connected to the control lines and the N bidirectional data lines of the packet bus; wherein each of the first and second packet bus 430 (Fig. 4) includes: control lines for conveying control signals (Col. 5 lines 4-7 and Fig. 5); and N bidirectional data lines for conveying a command packet and for conveying a data packet including the M its of data, wherein each of A and M is greater than N, and wherein A, M, and N are integers

(it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore A and M is greater than N); Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above. Funk et al. fails to clearly teach where there is address lines even though it is pretty well known as explained above. Funk further fails to teach a first and second master controller.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more A address (Col. 8 lines 37-38, there is address lines as being the "other signal lines") and M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2). Also, lines 1.17 (Fig. 2) are in parallel, so the address and data lines are in parallel.

Funk and Dias fail to teach address lines and a first and second master controller.

Woods's system teaches A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel (Col. 1 lines 60-62 and Col. 4 lines 3-7). Woods further teaches a first master controller 60 (Fig. 2), electrically connected to A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of a first packet bus for controlling via the first packet bus at least one peripheral 62 (Fig. 2) on the first packet bus; and a second master controller 50 (Fig. 2), electrically connected to the control lines and N bidirectional data lines of the second packet bus

the memory 75 (Fig. 2) shared by the modulator/demodulator 90 (Fig. 2) and by the central processing unit 25 (Fig. 2).

Regarding claim 35, Funk et al. teaches wherein the master controller controls the plurality of peripherals 101 and 425 (Fig. 4) by issuing a command packet commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) on the first packet bus 432, and 434 (Fig. 4), the command packet includes a module device select signal for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 36, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the command packet (Col. 7 lines 48-54).

Regarding claim 40, Funk et al. teaches controlling the master controller 111 (Fig. 4) via a processor bus 430, 432, and 434 (Fig. 4), wherein the A address lines convey A bits of an address in parallel and M data lines convey M bits of data in parallel (it is pretty well know there is address lines since the modem is being connected to a computer and in figure 4 shows the lines being in parallel); using the master controller 111 (Fig. 4, Col. 3 lines 26-30) to control a plurality of peripherals 425 (Fig. 4) including the signal modulator/demodulator 409 and 417 (Fig. 4) by issuing command packets via a packet bus 432 and 430 (Fig. 4) operatively connected to the master controller 111 (Fig. 4) and to each of the plurality of peripherals 409, 417, and 425 (Fig. 4), wherein the packet bus is characterized by having: control lines for conveying control signals (Col. 5 lines 4-7 and Fig. 5); and N bidirectional data lines for conveying a command

packet and for conveying a data packet including the M its of data, wherein each of A and M is greater than N, and wherein A, M, and N are integers (it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore A and M is greater than N). Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above. Also, Funk et al. fails to clearly teach where there is address lines even though it is pretty well known as explained above.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more A address (Col. 8 lines 37-38, there is address lines as being the "other signal lines") and M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2). Also, lines 1.17 (Fig. 2) are in parallel, so the address and data lines are in parallel.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate M data lines is greater than N data lines as taught by Dias et al. into Funk et al. wireless packet data communication modem in order to have a more compact circuit (Col. 7 lines 25-30).

Funk and Dias fail to teach address lines

Woods's system teaches A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel (Col. 1 lines 60-62 and Col. 4 lines 3-7).

Regarding claim 44, Funk et al. teaches wherein the step of controlling the plurality of peripherals includes issuing a command packet commonly receivable by the plurality of peripherals 101 and 425 (Fig. 4) over the packet bus 430, 432, wherein 434 (Fig. 4), the command packet includes a module device select signal for selecting one of the peripherals (Col. 3 lines 10-31 and Col. 4 lines 52-63).

Regarding claim 45, Funk et al. teaches wherein the selected one of the peripherals returns a signal to the master controller to acknowledge receipt (ARQ protocol) of the command packet (Col. 7 lines 48-54).

3. Claims 3-4, 7, 9, 11-12, 14-16, 18, 22-23, 27-28, 32, 37, 41, 46, and 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Woods et al. (US Pat# 6,101,566) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152).

Regarding claim 3, Funk et al. wireless packet data communication modem in view of Dias et al. circuit and further in view of Woods's system teaches the limitations in claim 1. Funk et al. and Dias et al. fails to teach about a memory shared by the modem and the master controller.

Gibbs et al. wireless trickle sync device teaches a shared memory 30 (Fig. 1) operatively connected to the modem 50 (Fig. 1) and the master controller 20 (Fig. 1) for access by either the modem 50 (Fig. 1) or the central processing unit 40 (Fig. 1).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate address lines as taught by Woods into a memory shared by the modem and the master controller as

taught by Gibbs et al. into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to reduce power consumption (Section 0002).

Regarding claim 4, Gibbs further teaches it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate SDRAM memory into Gibbs memory in order to provide small size, light weight, and low costs (Col. 2 lines 29-33).

Regarding claim 7, Gibbs et al. further teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1). Gibbs fails to teach a field that specifies length.

Funk teaches a field that specifies the length of a data packet (Fig. 5); and a field that indicates the start address of the commanded data (Fig. 5).

Regarding claim 9, Funk further teaches a first signal line for conveying a first control signal that indicates that the N bidirectional data lines currently carry a command packet or a data packet; and a second signal line for conveying a second control signal that indicates the current transfer direction over the N bidirectional data lines; and a forward clock line for conveying a control signal for synchronizing write-data packets (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Regarding claim 11, Funk et al. wireless packet data communication modem teaches a central processing unit 421 (Fig. 4) electrically connected to A address lines

and M data lines of a processor bus 430, 432, and 434 (Fig. 4), wherein the A address lines convey A bits of an address in parallel (it is pretty well know there is address lines since the modem is being connected to a computer and in figure 4shows the lines being in parallel) and the M data lines convey M bits of data in parallel (Fig. 5 shows that packet data is sent though the bus to the controller interface); a signal modulator/ demodulator 409 and 417 (Fig. 4), for effecting radio communications, a first packet bus 430 (Fig. 4) having: control lines for conveying control signals (Col. 5 lines 4-7 and Fig. 5); and N bidirectional data lines for conveying a command packet and for conveying a data packet including the M its of data, wherein each of A and M is greater than N, and wherein A, M, and N are integers (it is pretty well known that a logic unit 107 (Fig. 4) is smaller compared to the processor 421 (Fig. 4) unit therefore A and M is greater than N); a second packet bus 432 (Fig. 4) having control lines and N data lines for conveying a command packet and a data packet including the M bits of data; and a master controller 111 (Fig. 4, Col. 3 lines 26-30), electrically connected to the A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of the packet bus, for controlling via the packet bus a plurality of peripherals 425 (Fig. 4) electrically connected to the control lines and the N bidirectional data lines of the packet bus. Funk et al. fails to clearly teach were M data lines is greater than N data lines even though it pretty well known as explained above. Funk et al. fails to clearly teach where there is address lines even though it is pretty well known as explained above. Funk further fails to teach a first and second master controller and memory shared by a demodulator/modulator.

Dias et al. circuit teaches a control logic unit 1.30 (Fig. 1.2) and a processor 1.14 (Fig. 1.2). It is shown that there are many more A address (Col. 8 lines 37-38, there is address lines as being the "other signal lines") and M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2). Also, lines 1.17 (Fig. 2) are in parallel, so the address and data lines are in parallel.

Funk and Dias fail to teach address lines, a first and second master controller, and memory shared by a demodulator/modulator.

Woods's system teaches A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel (Col. 1 lines 60-62 and Col. 4 lines 3-7). Woods further teaches a first master controller 60 (Fig. 2), electrically connected to A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of a first packet bus for controlling via the first packet bus at least one peripheral 62 (Fig. 2) on the first packet bus; and a second master controller 50 (Fig. 2), electrically connected to the control lines and N bidirectional data lines of the second packet bus the memory 75 (Fig. 2) shared by the modulator/demodulator 90 (Fig. 2) and by the central processing unit 25 (Fig. 2).

Funk et al., Woods, and Dias et al. fail to teach memory shared by a demodulator/modulator.

Gibbs et al. wireless trickle sync device teaches a memory 30 (Fig. 1) shared by the modulator/demodulator 50 (Fig. 1) and the central processing unit 40 (Fig. 1).

Regarding claim 12, Woods further teaches wherein the second master controller 50 (Fig. 2) is electrically connected to the A address lines and M data lines of the processor bus 27 (Fig. 2) and further controls a flash memory 75 (Fig. 2) via the control lines and N bidirectional data lines of the second packet bus.

Regarding claim 14, Woods further teaches wherein the first master controller 60 (Fig. 2) controls the plurality of peripherals 62 (Fig. 2) operatively connected to the first packet bus by issuing a command packet commonly receivable by the plurality of peripherals over the N bidirectional data lines of the first packet bus 430 (Fig. 4), the command packet includes a module device select signal for selecting one of the peripherals.

Regarding claim 15, Funk et al. further teaches wherein the selected one of the plurality of peripherals returns a signal over the control lines of the first packet bus to the master controller to acknowledge receipt (ARQ protocol) of the command (Col. 7 lines 48-54).

Regarding claim 16, Gibbs et al. further teaches wherein the packetized command includes a read/write command (SRAM, Section 0013) to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1). Gibbs fails to teach a field that specifies length.

Funk teaches a field that specifies the length of a data packet (Fig. 5); and a field that indicates the start address of the commanded data (Fig. 5).

Regarding claim 18, Funk further teaches wherein M is an integer multiple of N (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Figs. 4-5).

Regarding claim 19, Funk further teaches wherein N is four (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Regarding claim 20, Funk further teaches a signal line that indicates whether the N bidirectional data lines currently carry a command packet or a data packet; a signal line that indicates the current transfer direction over the N bidirectional data lines (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Regarding claim 22, Gibbs et al. further teaches a shared memory 30 (Fig. 1) electrically connected to the modem 50 (Fig. 1) and the master controller 20 (Fig. 1) for access by either the modem 50 (Fig. 1) or the central processing unit 40 (Fig. 1).

Regarding claim 23, Woods further teaches a second master controller 50 (Fig. 2) and the shared memory 75 (Fig. 2) and the second master controller are operatively connected to each other via a second bus 27 (Fig. 2) having: control lines for conveying control signals; and N bidirectional data lines for conveying a command packet and for conveying data packets.

Regarding claim 27, Gibbs et al. further teaches wherein the command packet includes a field specifying a read/write command (SRAM, Section 0013). Gibbs fails to teach a field that specifies length.

Funk teaches a field that specifies the length of a data packet (Fig. 5); and a field that indicates the start address of the commanded data (Fig. 5).

Regarding claim 28, Funk teaches wherein the command packet includes a module device select signal used for selecting one of the peripherals (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 4).

Regarding claim 32, Gibbs further teaches a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and by the central processing unit 40 (Fig. 1).

Regarding claim 37, Gibbs further teaches wherein the command packet includes a read/write command (SRAM, Section 0013) directed to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1).

Regarding claim 38, Funk teaches a field that specifies the length of a data packet (Fig. 5); and a field that indicates the start address of the commanded data (Fig. 5).

Regarding claim 41, the combination including Gibbs et al. teaches about a memory 30 (Fig. 1) shared by the modem 50 (Fig.1) and the central processing unit 40 (Fig. 1).

Regarding claim 46, Gibbs et al. further teaches wherein the command packet includes a read/write command (SRAM, Section 0013) directed to a memory 30 (Fig. 1) shared by the modem 50 (Fig. 1) and the central processing unit 40 (Fig. 1).

Regarding claim 49, Woods further teaches wherein the second master controller is in the modulator/demodulator (Fig. 2).

Regarding claim 50, Woods further teaches wherein the first master controller 60 (Fig. 2) and the second master controller 50 (Fig. 2) are electrically connected to the A address lines and M data lines of the processor bus 55 (Fig. 2).

4. Claims 4, 24, 34, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat#

5,010,331) and further in view of Woods et al. (US Pat# 6,101,566) and further in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 4, Funk et al. wireless packet data communication modem in view of Dias et al. circuit teaches the limitations in claim 1 and wherein the plurality of peripherals include at least one of an a display 425 (Fig. 4) of Funk et al. reference. Funk et al. and Dias et al. fails to teach a plurality of peripherals include at least one of an image capture module and a flash memory.

Wilska et al. device for personal communications teaches wherein the plurality of peripherals operatively connected to the bus include the modem 17 (Fig. 3) and at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a plurality of peripherals include at least one of an image capture module and a flash memory as taught by Wilska et al. into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

Regarding claim 24, Wilska et al. further teaches wherein the plurality of peripherals additionally include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Regarding claim 34, Wilska et al. teaches wherein the plurality of peripherals include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

Regarding claim 43, Wilska et al. teaches wherein the plurality of peripherals include at least one of an image capture module 14 (Fig. 3), a display 9 (Fig. 3), and a flash memory 13 (Fig. 3).

5. Claims 8, 17, 29, 33, 39, 42, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Woods et al. (US Pat# 6,101,566) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152) and further Watanabe et al. (US Pat# 6,378,102).

Regarding claim 8, Funk et al. wireless packet data communication modem in view of Dias et al. circuit and further in view of Gibbs et al. wireless trickle sync device teaches the limitations in claims 1, 5, and 7. Funk et al., Dias et al. and Gibbs et al. fail to teach about a strobe signal.

Watanabe et al. synchronous semiconductor memory device with multi-bank configuration teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a strobe signal as taught by Watanabe et al. into a memory shared by the modem and the master

controller as taught by Gibbs et al. into address lines as taught by Woods into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to have faster operation (Col. 2 lines 4-10).

Regarding claim 17, Watanabe et al. further teaches data read from the memory is transmitted out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 29, Watanabe et al. further teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

Regarding claim 33, the combination including Gibbs. teaches it would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate SDRAM memory into Gibbs memory in order to provide small size, light weight, and low costs (Col. 2 lines 29-33).

Watanabe et al. further teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6).

Regarding claim 39, Funk further teaches wherein the control lines of the first packet bus includes a signal line that indicates whether the N bidirectional data lines currently carry a command packet or a data packet; a signal line that indicates the

current transfer direction over the N bidirectional data lines (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Regarding claim 42, Watanabe et al. further teaches wherein the SDRAM includes a plurality of data banks (Col. 2 lines 20-24) and an interface for interfacing the master controller (Col. 26 lines 1-6). Watanabe fails to teach a first and second master controller.

Woods further teaches a first interface 50 (Fig. 2) for interfacing the master controller via the N bidirectional data lines of the packet bus 27, 17, and 55 (Fig. 2), and a second interface 100 (Fig. 2) for interfacing a second master controller in the modulator/demodulator 90 (Fig. 2) via the N bidirectional data lines of a second packet bus 87 (Fig. 2).

Regarding claim 47, Watanabe further teaches wherein data read from the memory is transmitted out externally with a strobe signal, the strobe signal is for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

6: Claim 10 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Woods et al. (US Pat# 6,101,566) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152) and further Fueki (US Pat Appl# 2002/0166058).

Regarding claim 10, Funk et al. wireless packet data communication modem in view of Dias et al. circuit and further in view of Gibbs et al. wireless trickle sync device

teaches the limitations in claims 1, 2, and 3. Funk et al., Dias et al. and Gibbs et al. fail to teach a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into a memory shared by the modem and the master controller as taught by Gibbs et al. into address lines as taught by Woods into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to increase security (section 0015).

Regarding claim 48, Fueki teaches wherein the memory includes a protection circuit for receiving address data from an external devices and for generating a protect signal upon simultaneously receiving the same address from external devices (Sections 0014 and 0031).

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Woods et al. (US Pat# 6,101,566) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claim 11 above, and further in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 13, Funk et al. in view of Dias et al. and further in view of Woods and further in view of Gibbs et al. teaches the limitations in claim 11. Funk et al., Dias et al., Woods, and Gibbs et al. fail to teach an image capture module.

Wilska et al. device for personal communications teaches wherein the at least one peripheral is an image capture module 14 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate an image capture module as taught by Wilska et al. into a memory shared by the modem and the master controller as taught by Gibbs et al. into address lines and a first and second controller as taught by Woods into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

8. Claims 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Funk et al. (US Pat# 6,026,119) in view of Dias et al. (US Pat# 5,010,331) and further in view of Woods et al. (US Pat# 6,101,566) and further in view of Gibbs et al. (US Pat Appl# 2003/0114152) as applied to claims 11 and 18 above, and further in view of Fueki (US Pat Appl# 2002/0166058).

Regarding claim 20, Funk et al. in view of Dias et al. and further in view of Gibbs et al. teaches the limitations in claims 11 and 18. Funk et al., Dias et al., and Gibbs et al. fail to teach a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a protection circuit for receiving address data

from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into a memory shared by the modem and the master controller as taught by Gibbs et al. into M data lines is greater than N data lines as taught by Funk et al. in view of Dias et al. circuit in order to increase security (section 0015).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Wendell whose telephone number is 571-272-0557. The examiner can normally be reached on 7:30-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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11/17/2006

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